ADSP-21161N BOM Change Summary

ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

	Stats Singapore - STA *(From)*	**Stats Korea – SK3** *(To)*
D/A	Ablestik 2000 conductive	Ablestik 2000B conductive
Wire	Au / 1.0 mil	Au / 1.0 mil
EMC	G770	KE-G2280TS
Ball Composition	96.5Sn_3.0Ag_0.5Cu	96.5Sn_3.0Ag_0.5Cu

Qualification Plan Summary for CSP_BGA at STATS ChipPAC Korea

TEST	SPECIFICATION	SAMPLE SIZE	EXPECTED COMPLETION DATE
Temperature Cycle (TC)*	JEDEC *JESD22-A104*	3 x 77	Oct 2020
Solder Heat Resistance (SHR)*	JEDEC/IPC *J-STD-020*	3 x 11	Oct 2020
Temperature Humidity Bias (THB)*	JEDEC *JESD22-A101*	3 x 77	Oct 2020
High Temperature Storage (HTS)	JEDEC *JESD22-A103*	1 x 45	Oct 2020
Unbiased Highly Accelerated Stress Test (UHAST)*	JEDEC *JESD22-A118*	3 x 77	Oct 2020

* These samples will be subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: 1. Bake – 24 hours at 125°C; 2. Soak – unbiased soak for 192 hours at 30°C, 60%RH; 3. Reflow – three passes through a reflow oven with a peak temperature of 260°C. TC samples will be subjected to wire-pull test after 500 cycles where results should be within specification limits.